the source and the N channel to the drain. The representation is the same as for D2 and D4 in Figs. 3 and 5. For P channel transistors, the bulk diodes have a reverse polarity from the body to the drain, which is properly represented as D1 and D3 in Figs. 3 and 5. Since the diodes are properly illustrated, the charge can pass through the bridge. With the diodes as illustrated in Figs. 3 and 5, the output charge would rise to the value set forth in equation [1] in the specification. Accordingly, the specification is enabling, and the objection to the specification and rejection of claims 1-25 under 35 U.S.C. § 112, first paragraph should be withdrawn.

The claims have been amended to correct the errors noted in the Office Action and other errors noted by applicants. Applicants respectfully suggest that the language relating to the bridges of diodes and transistors is correct. Claims 2 and 9 recite MOS transistors connected in a manner to create a one-way conduction path between the negative and positive terminals of the inverters. As illustrated in the Figs. 3 and 5 (and discussed in the specification), the bridge includes two N-channel and two P-channel transistors. The transistors are formed in a bridge arrangement and controlled in a way which results in a one way conduction path from the negative terminal to the positive terminal of the bridge. The bulk diodes do not result in conduction in an opposite direction. Thus, the claims properly recite the arrangement illustrated in the drawings, and are correct. Also, the recitation of four diodes and four transistors is proper. It is possible to use distinct elements. Also, claim 5 properly recites that the diodes are bulk diodes of the transistors. Thus, the diodes may be formed by the same process which forms the transistors, but do not need to be. Accordingly, the claims properly recite the elements as being

the same and separate.

Applicants respectfully traverse the rejection of claims 1-25 under 35 U.S.C. § 103 as being unpatentable over Matsumura or Okada. The Office Action notes significant differences between the circuits shown in Matsumura or Okada. For example, neither reference teaches or suggests two inverters, a bridge circuit of four diodes, four transistors having conduction paths parallel with the diodes, or a charge accumulation condenser. Furthermore, neither reference teaches or suggests a negative input connected to a continuous power voltage. The Office Action merely asserts, without any support or basis, that one would necessarily change the diode connected transistors to switching transistors in order to reduce the voltage loss. However, there is no suggestion in either reference that such a change could be made, or how to make such a change.

Applicants respectfully suggest that the changes necessary to convert the circuits in the cited art into the circuits recited in the present claims are significant and are not suggested by the references or information known in the art. As discussed in the present application, different types of MOS transistors can be connected in a bridge circuit to form two inverters. Both Matsumura and Okada disclose four P channel transistors. No N channel transistors are used in either reference. Additionally, although the diodes could be replaced with switching transistors, the cited art does not teach how such transistors should be switched or connected to the transistors already in the circuit. Merely eliminating the connection between the base and drain would not create a switched transistor and would not result in a voltage doubler, as recited in the

claims. The electrical connections of the transistors and diodes is necessary in order to achieve proper operation as a voltage doubler. Thus, the recitations in the claims of the connections of the inverters (claim 1), diodes (claim 3), and switches (claims 6, 13, 14, 19, 24 and 25) are necessary to proper operation of the circuit. These connection are not suggested by the cited art, even if the diodes in the cited art were changed to switching transistors.

Additionally, as noted above, neither of the cited references includes a circuit which has a negative terminal connected to a continuous power voltage and an positive terminal connected to a output of the voltage doubler, as recited in the claims. Therefore, neither reference teaches or suggests how it could be modified to obtain the claims invention.

Therefore, claims 1-25 patentably distinguish over the cited art and are in condition for allowance.

Finally, claim 25 recites a method in which a plurality of bridge circuits connected in series are used to generate an increased voltage. Neither reference suggests that multiple bridge circuits (even if they were to suggests a single bridge circuit recited in the claims) could be used to generate increased voltages. Thus, claim 25 further distinguishes over the cited art and is in condition for allowance.

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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